UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,663	11/28/2000	Farhad Fouladi	723-963	5292

27562 7590 04/10/2006

NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
WANG, JIN CHENG	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,663	FOULADI ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7,11,17,19-22 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7, 11, 17, 19-22, 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/7/2006 has been entered. Claims 5-7, 11, 17, 19-22, 24 have been amended. Claims 25-26 are newly added. Claims 1-4, 8-10, 12-16, 18 and 23 have been canceled. Claims 5-7, 11, 17, 19-22, 24-26 are pending in the application.

Response to Arguments

1. Applicant's arguments with respect to claims 5-7, 11, 17, 19-22, 24-26 have been considered but are moot in view of the new ground(s) of rejection based on unpatentable over Chen U.S. Pat. No. 6,532,018 (hereinafter Chen) in view of Migdal et al. U.S. Patent No. 6,426,753 (hereinafter Migdal).

For example, Chen discloses M chip memory organization (the copy-out pipeline M0) which permits very fast copying of data from the embedded frame buffer memory to texture memory wherein the data is repacked into a selected texture format before and during copying out to the texture memory (*e.g., column 2, lines 28-49; column 3, lines 4-42; column 4, lines 48-67; column 5, lines 1-12*). It is not clear whether the content of the embedded frame buffer memory of one M-chip can be copied to the frame buffer memory or the texture memory of the other M-chip. However, Migdal discloses data from one M chip is accessible to another M chip

over an internal network (Migdal col. 6), i.e., *the texture data in the frame buffer memory of one M chip can be requested and routed to the texture memory buffer of another M chip* (Migdal col. 6).

It would have been obvious to one of the ordinary skill in the art to have incorporated into Migdal's teachings that data from one M chip can be requested and routed to another M chip (main memory resident on another M chip) because Chen teaches a plurality of M chips within his graphics system (Chen Figs. 1-3) and the embedded frame buffer and texture buffer with each of the M chips and Chen suggests the logic processing operations within the logic core and copying operations of data from frame buffer memory to texture memory (Chen column 2-4) and therefore Chen suggests the copying out operations from the frame buffer memory of one M chip to the memory units of another M chip including the frame buffer area and texture buffer area of the M chip (Chen column 2-4).

In view of the teaching of Midgal, Chen's M chip memory organization (copy-out pipeline of the M-chip M0) is operable to selectively transfer the data to either a display buffer area or a texture buffer area with said main memory resident on another M-chip such as M-chip M1 (*e.g., Chen Figures 1-3; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12; Migdal col. 6*).

Chen further disclose the claimed limitation of the copy pipeline converting the data to a display format if the data is transferred to the display buffer and a texture format if the data is transferred to the texture buffer (*e.g., Chen Figures 1-3; column 2, lines 28-49;* ***column 4, lines 48-67; column 5, lines 1-45****; Migdal col. 6*).

One of the ordinary skill in the art would have been motivated to incorporate Migdal's teaching because the texture data or the display data in the frame buffer memory of one M chip can be requested and routed to the texture memory buffer of another M chip (Migdal col. 6).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 25 and 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim 25 recites "non-embedded main memory". The meaning of "non-embedded" is not clear. Clarification is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25, 5-7, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen U.S. Pat. No. 6,532,018 (hereinafter Chen) in view of Migdal et al. U.S. Patent No. 6,426,753 (hereinafter Migdal).

4. Claim 25:

(a) Chen teaches a graphics system including a main processor and a graphics coprocessor having an embedded frame buffer, comprising:

A graphics coprocessor having an embedded frame buffer (The DRAM graphics coprocessor having a logic core and memory units, for example, the M-chip M0; see also column 3, lines 4-19);

A main memory on a separate chip from said graphics coprocessor (*e.g., memory units on a different and separate chip or M-chip because of the presence of a plurality of M chips, for example, the main memory on the M-chip M1; Figs. 1-3; col. 2-3*);

A copy pipeline on said graphics coprocessor which transfers data from the embedded frame buffer (*the embedded frame buffer of Figure 3 within the M-chip M0*) to the non-embedded main memory (*e.g., the main memory can be the texture memory within the memory units of a M-chipor the registers/buffers resident on the rasterizer chip, which is TRULY non-embedded within the M-chip M0. See Figures 1-3; column 2; column 4, lines 48-67; column 5, lines 1-12*);

(b) It is not clear whether Chen discloses the claim limitation of "A pixel data post-processing copy-out pipeline that selectively converts pixel data from one image format to another during a reading and transfer of the data from the embedded frame buffer to a separate non-embedded main memory of said graphics system, wherein the copy-out pipeline is operable to selectively transfer the data to either a display buffer area or a texture buffer area within said main memory and wherein the copy-out pipeline converts the data to a display format if the data

is transferred to the display buffer area and converts the data to a texture format if the data is transferred to the texture buffer area."

(c) Chen discloses M chip memory organization (the copy-out pipeline M0) which permits very fast copying of data from the embedded frame buffer memory to texture memory wherein the data is repacked into a selected texture format before and during copying out to the texture memory (*e.g., column 2, lines 28-49; column 3, lines 4-42; column 4, lines 48-67; column 5, lines 1-45*). It is not clear whether the content of the embedded frame buffer memory of one M-chip can be copied to the frame buffer memory or the texture memory of the other M-chip. However, Migdal discloses data from one M chip is accessible to another M chip over an internal network (Migdal col. 6), i.e., *the texture data in the frame buffer memory of one M chip can be requested and routed to the texture memory buffer of another M chip* (Migdal col. 6).

(d) It would have been obvious to one of the ordinary skill in the art to have incorporated into Migdal's teachings that data from one M chip can be requested and routed to another M chip (main memory resident on another M chip) because Chen teaches a plurality of M chips within his graphics system (Chen Figs. 1-3) and the embedded frame buffer and texture buffer with each of the M chips and Chen suggests the logic processing operations within the logic core and copying operations of data from frame buffer memory to texture memory (Chen column 2-4) and therefore Chen suggests the copying out operations from the frame buffer memory of one M chip to the memory units of another M chip including the frame buffer area and texture buffer area of the M chip (Chen column 2-4).

In view of the teaching of Midgal, Chen's M chip memory organization (copy-out pipeline of the M-chip M0) is operable to selectively transfer the data to either a display buffer

area or a texture buffer area with said main memory resident on another M-chip such as M-chip M1 (*e.g., Chen Figures 1-3; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12; Migdal col. 6*).

Chen further disclose the claimed limitation of the copy pipeline converting the data to a display format if the data is transferred to the display buffer and a texture format if the data is transferred to the texture buffer (*e.g., Chen Figures 1-3; column 2, lines 28-49;* ***column 4, lines 48-67; column 5, lines 1-45****; Migdal col. 6*).

(e) One of the ordinary skill in the art would have been motivated to incorporate Migdal's teaching because the texture data or the display data in the frame buffer memory of one M chip can be requested and routed to the texture memory buffer of another M chip (Migdal col. 6).

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 25 except additional claimed limitation that the graphics coprocessor further includes a graphics pipeline, wherein the graphics pipeline is operable to use the data copied out to the main memory texture buffer area in a subsequent rendering process.

However, Chen further discloses the claimed limitation that that the graphics coprocessor further includes a graphics pipeline, wherein the graphics pipeline is operable to use the data copied out to the main memory texture buffer area in a subsequent rendering process (*e.g., Figures 1-3 and column 1, lines 30-47;* ***column 4, lines 48-67; column 5, lines 1-45***).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 25 except additional claimed limitation that the copy pipeline selectively reads data from the embedded frame buffer in RGB color format or YUV color format. However, Chen further discloses the claimed limitation that the embedded frame buffer may be programmably configured to store pixel data in either RGB color format or YUV color format (*e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12*).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 25 except additional claimed limitation that the copy-out pipeline selectively converts the data from the embedded frame buffer to either a YUV display format or an RGB texture format during a copy out of pixel data to the external frame buffer in main memory. However, Chen and Migdal further disclose the claimed limitation that the copy-out pipeline selectively converts the data from the embedded frame buffer to either a YUV display format or an RGB texture format during a copy out of pixel data to the external frame buffer in main memory (*e.g., the main memory being resident to another M-chip is therefore "external" to the different M-chip M0 meaning a "copy-out" operation. Chen Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12; Migdal col. 6*).

Re Claim 24:

Chen discloses a graphics system, comprising:

Selecting a sub-region of pixels in the embedded frame buffer as a source for a pixel data transfer operation, then selectively performing **one or more of the following operations** on

pixel data selected for transfer from said embedded frame buffer to said external frame buffer (***column 4, lines 48-67; column 5, lines 1-45***);

Antialiasing and/or delicker filtering using pixel data sample from one or more rows of pixel data stored in said embedded frame buffer (**column 3, lines 54-67 and column 4, lines 1-7 and column 1, lines 48-60; column 5, lines 1-45**);

Gamma correction of pixel data stored in said embedded frame buffer (**column 3, lines 54-67 and column 4, lines 1-7**);

Converting pixel data stored in said embedded frame buffer in RGB format to YUV format (*Figs. 4a and 4b*);

Scaling the vertical display size of pixel data stored in said embedded frame buffer (column 3, lines 54-67);

Selecting a destination in the external frame buffer for the pixel data transfer operation (**column 3, lines 54-67 and column 4, lines 1-7 and column 1, lines 48-60**).

Chen discloses M chip memory organization (the copy-out pipeline M0) which permits very fast copying of data from the embedded frame buffer memory to texture memory wherein the data is repacked into a selected texture format before and during copying out to the texture memory (*e.g., column 2, lines 28-49; column 3, lines 4-42; column 4, lines 48-67; column 5, lines 1-12*). It is not clear whether the content of the embedded frame buffer memory of one M-chip can be copied to the frame buffer memory or the texture memory of the other M-chip. However, Migdal discloses data from one M chip is accessible to another M chip over an internal network (Migdal col. 6), i.e., *the texture data in the frame buffer memory of one M chip can be requested and routed to the texture memory buffer of another M chip* (Migdal col. 6).

It would have been obvious to one of the ordinary skill in the art to have incorporated into Migdal's teachings that data from one M chip can be requested and routed to another M chip (main memory resident on another M chip) because Chen teaches a plurality of M chips within his graphics system (Chen Figs. 1-3) and the embedded frame buffer and texture buffer with each of the M chips and Chen suggests the logic processing operations within the logic core and copying operations of data from frame buffer memory to texture memory (Chen column 2-4) and therefore Chen suggests the copying out operations from the frame buffer memory of one M chip to the memory units of another M chip including the frame buffer area and texture buffer area of the M chip (Chen column 2-4).

In view of the teaching of Midgal, Chen's M chip memory organization (copy-out pipeline of the M-chip M0) is operable to selectively transfer the data to either a display buffer area or a texture buffer area with said main memory resident on another M-chip such as M-chip M1 (*e.g., Chen Figures 1-3; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12; Migdal col. 6*).

Chen further disclose the claimed limitation of the copy pipeline converting the data to a display format if the data is transferred to the display buffer and a texture format if the data is transferred to the texture buffer (*e.g., Chen Figures 1-3; column 2, lines 28-49;* ***column 4, lines 48-67; column 5, lines 1-45****; Migdal col. 6*).

One of the ordinary skill in the art would have been motivated to incorporate Migdal's teaching because the texture data or the display data in the frame buffer memory of one M chip can be requested and routed to the texture memory buffer of another M chip (Migdal col. 6).

5. Claims 11 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen U.S. Pat. No. 6,532,018 (hereinafter Chen) as applied to claim 1 above, and further in view of Migdal et al. U.S. Patent No. 6,426,753 (hereinafter Migdal), Nally et al. U.S. Patent No. 5,506,604 (hereinafter Nally).

6. Claim 11:

(1) Chen and Midgal have taught the claim limitation as recited in claim 25 and 24.

(2) However, it is silent on converting the image data from YUV color format to RGB color format or vice versa.

(3) However, Nally teaches converting the image data from YUV color format to RGB color format or vice versa (Nally column 5, lines 1-67; column 6, lines 1-59).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Nally's teachings into the Chen and Migdal's method and system of transferring data from a graphics chip to a main memory because Chen suggests a display chip which directs the rasterizer chip what data to retrieve from the frame buffer and provides some formatting of the data before sending it to the display chip for data to be displayed on a monitor (Chen column 2, lines 30-50) as well as COLOR CONVERSIONS (Figs. 4a and 4b) and therefore suggesting an obvious modification.

(5) Therefore, it would have been obvious to have incorporated Nally's decoding and encoding circuitry because it facilitates logic for color conversion from scaling/zooming of the incoming video and graphics data in the frame buffer.

Claim 21:

The claim 21 encompasses the same scope of invention as that of claim 26 except additional claimed limitation of performing an anti-aliasing operation on the data prior to converting the image data to YUV format and writing the image data to the frame buffer located in main memory of the graphics system. However, Chen further discloses the claimed limitation of performing an anti-aliasing operation on the data prior to converting the image data to YUV format and writing the image data to the frame buffer located in main memory of the graphics system (**e.g., column 5, lines 1-45**).

7. Claims 17, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen U.S. Pat. No. 6,532,018 (hereinafter Chen) as applied to claim 1 and 12 above, and further in view of Nally et al. U.S. Patent No. 5,506,604 (hereinafter Nally) and Nakamura et al. U.S. Patent No. 6,384,831 (hereinafter Nakamura).

8. Claims 17, 19, 20 and 22:

(1) Chen AND Midgal have taught the claim limitation as recited in claim 26.

(2) However, it is silent on converting the image data from YUV color format to RGB color format or vice versa; the display format being a YUV 4:2:2 format and performing a scaling/gamma correction/de-flickering operation on the image data.

(3) However, Nally teaches converting the image data from YUV color format to RGB color format or vice versa; the display format being a YUV 4:2:2 format and performing a scaling operation on the image data (Nally column 5, lines 1-67; column 6, lines 1-59) and

performing a de-flickering/gamma correction operation on the image data (Nakamura the abstract).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Nally and Nakamura's teachings into the Chen and Migdal's method and system of transferring data from a graphics chip to an external image storage location because Chen suggests a display chip which directs the rasterizer chip what data to retrieve from the frame buffer and provides some formatting of the data before sending it for data to be displayed on a monitor (Chen column 2, lines 30-50) and therefore suggesting an obvious modification.

(5) Therefore, it would have been obvious to have incorporated Nally's decoding and encoding circuitry because it facilitates logic for color conversion from scaling/zooming of the incoming video and graphics data in the frame buffer and Nakamura's image processing operation so that desired image effect can be obtained.

Conclusion

The claims 24 and 26 are also rejected under 102(e) as being anticipated by Yasumoto, U.S. Patent No. 6,747,642 (hereinafter Yasumoto). Yasumoto discloses a graphics system, comprising: Selecting a sub-region of pixels in the embedded frame buffer as a source for a pixel data transfer operation, then selectively performing one or more of the following operations on pixel data selected for transfer from said embedded frame buffer to said external frame buffer (*The cited reference discloses selecting and processing the pixels around the object edges or the pixels associated with the cartoon character; column 8, lines 53-67 and column 9-10*); Antialiasing and/or delicker filtering using pixel data sample from one or more rows of pixel data stored in said embedded frame buffer (*the cited reference discloses a pixel filtering routine within the pixel filter 50 performing a pixel post-processing for pixels for pixels shown in Fig. 2A having at least one or more rows of pixel data stored in said embedded frame buffer 1126a shown in Fig. 1D; see column 8-10; wherein antialiasing includes modifying the color and transparency values and dithering the depth data of the pixels*); Gamma correction of pixel data stored in said embedded frame buffer (*the blending coefficients of pixels undergo alpha correction to compensate for the gamma or the gray-scale values in the pixel rendering/filtering processes. The alpha correction includes selecting a set of correction coefficients and computing*

corrected alpha values and the corrected alpha values are used to blend the foreground and background colors of the display pixels; column 9-10); Converting pixel data stored in said embedded frame buffer in RGB format to YUV format (*converting the RGB pixel data to YUV pixel data may also be applied in the pixel filter; see column 10, lines 33-40*); Scaling the vertical display size of pixel data stored in said embedded frame buffer (*Scaling includes the perspective translation of the pixels which affects the vertical size of the display pixels and the distance relative to the viewpoint for each pixel or sub-pixel stored in the frame buffer is changed. As the object relative distance is changed, the vertical display size of the pixel data for the associated object is accordingly changed; see column 10*); Selecting a destination in the external frame buffer for the pixel data transfer operation (*e.g., column 6, lines 1-11*).

Yasumoto also discloses a graphics system, including: A main processor (e.g., Figs. 1 and 1D); a graphics coprocessor having an embedded frame buffer (e.g., Figs. 1 and 1D and column 6, lines 1-11); A main memory on a separate chip from said graphics coprocessor (e.g., the off-chip main memory 1030 for access by an on-chip display unit 1128; see Figs. 1D and column 6, lines 1-11); a copy pipeline on said graphics coprocessor which transfers data from the embedded frame buffer to said main memory (e.g., the graphics pipeline 1116 may include an embedded DRAM memory 1126a to store frame buffer information locally. The on-chip frame buffer 1126a is periodically written to an off-chip main memory 1030 for access by an on-chip display unit 1128; see Fig. 1D and column 6, lines 1-11); Wherein the copy pipeline converts the data from one format to another format after reading the data from the embedded frame buffer and during transfer of the data from the embedded frame buffer to the main memory (e.g., pixel filter 50 may operate to apply border line cartoon outlining during this written process and thereby disclosing changing the formats of the graphics data during the written process or during the copying process of writing the graphics data from the on-chip frame buffer to the off-chip main memory. The pixel filter 50 reads data from the on-chip frame buffer. See Fig. 1D and column 6, lines 1-11. Moreover, in column 5, lines 40-67, Yasumoto discloses the graphics pipeline 1116 having the transform unit 1118, a setup rasterizer 1120, a texture unit 1122, a texture environment unit 1124 and a pixel engine 1126 in which the transform unit 1118 performs a variety of 3D transform operations and perform lighting and texture effects and the pixel engine 1126 performs z buffering, blending and stores data into an on-chip frame buffer memory). **In view of the prior art of record, the claim 24 and similar claims are proved to be unpatentable.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw